Remarks/Arguments

Summary

Claims 1 and 15 have been amended to provide a minor clarification. Claims 1-2, 4-9, 11-16, and 18-25 are currently pending in this application.

Objection to the Drawings

The Office Action objected to the drawings under 37 C.F.R. § 1.83(a), stating "the memory banks as recited in claims 4-5, 11-12, and 18-19 must be shown or the feature(s) canceled from the claims" (See, Office Action at page 2). Contrary to the Office Action's statement, exemplary memory banks are already shown by way of illustration in Figure 3B. The exemplary memory banks are labeled **B1** and **B2** and they are described, for example, on page 6, lines 24-29 of the specification.

As described on page 6 of the specification, Figure 3B shows one way of configuring memory modules 205, 207, 211, and 213 shown in Figure 2A. In particular, memory module 310 in Figure 3B shows 18 memory devices divided into two (2) banks. Thus, in the embodiment shown in Figure 3, L is equal to 18, and N is equal to 2. The width of a system bus connected to memory module 310 is 36 bits, i.e., 4x9 and therefore, since 36 = M/N, M is equal to 72 for this example. Further, each of the L devices shown in Figure 3B has a data bus width of 72/18, or M/L bits (See, e.g., claims 6, 13, and 20).

Since exemplary memory banks are clearly illustrated in Figure 3, the Office Action's objection to the drawings is inappropriate and should be withdrawn.

Claim Rejections - 35 U.S.C. § 102(b)

The Office Action rejected claims 1-2, 4-9, 11-16, and 18-25 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,466,496 to Kuge (hereafter, Kuge). These rejections are respectfully traversed for at least the following reasons.

The Office Action starts off by stating that Kuge discloses "system data buses DQ each having a multi-bit structure which may be 32-bit, therefore, each system data bus must inherently have a width of M bits." (See, Office Action at paragraph 3). Whether or not this statement is even true, it fails to address any specifically recited

element of any of the claims. For example, independent claims 1, 8, and 15 define "N system data buses having a width of M/N bits" – not a bus with a width of M bits. Absent a showing that Kuge discloses N system data buses, each with a width or M/N, the rejection of independent claims 1, 8, and 15 under 35 U.S.C. § 102(b) is improper and should be withdrawn.

The Office Action continues by asserting that Kuge discloses memory module groups 1000A, 1000B, and 1000C. (See, Office Action at paragraph 3). Since these so-called "memory module groups" are disclosed in Kuge, and also later in the Office Action, as simply "memory modules," it will be assumed that the Office Action is claiming that each memory module group includes only one memory module. Under such an interpretation, these so-called "memory module groups" would not read on any of the claims in the present application, because at least some module group in each claim contains N modules, where N is a natural number *greater than or equal to 2*.

Even if there existed some interpretation of Kuge under which the memory modules could be grouped to read on some of the claims, Kuge never discloses N system data buses respectively connected to N memory modules within a memory module group. Instead, data line DQ in Kuge is simply connected in substantially the same way to each of modules 1000A, 1000B, and 1000C. (See, Kuge at column 6, lines 12-15). This is completely different from the claims, which define memory module groups containing "N memory modules...respectively connected to the N system buses." Since Kuge fails to disclose the memory module groups defined by independent claims 1, 8, and 15, and similarly fails to disclose the associated bus interconnections, the rejection of independent claims 1, 8, and 15 under 35 U.S.C. § 102(b) is improper and should be withdrawn.

The Office Action further states that Kuge discloses "chip select signals /CS." (See, Office Action, paragraph 3). It appears that the Office Action equates chip select signals /CS in Kuge with various chip select signals defined in independent claims 1, 8, and 15. However, the Office Action ignores the fact that each of the module groups described above is operated in response to the chip select signals. Since Kuge does not disclose module groups as described above, the chip select

signals /CS in Kuge are different from the chip select signals defined by independent claims 1, 8, and 15. Since Kuge fails to disclose the chip select signals defined by any of independent claims 1, 8, and 15, the rejection of these claims under 35 U.S.C. § 102(a) is unwarranted and should be withdrawn.

Next, the Office Action argues that because Kuge discloses a method of measuring the length of data transmission lines in order to determine hold and set up times for memory chips in memory modules 1000A, 1000B, and 1000C, the set up/hold times for the modules *could* be set up to be the same. This argument has several major flaws, some of which are discussed below.

First, Kuge does not disclose measuring the length of any data transmission lines for modules within the same memory module group and controlled by the same chip select signal. Instead, Kuge discloses measuring the length of data transmission lines for individual modules, each controlled by a different chip select signal. In other words, Kuge does not even attempt to address the problem of relative data transmission times between memory modules *within the same memory module group* and a memory controller. Accordingly, Kuge utterly fails to disclose "N system buses wired such that data transmission times between the N memory modules within each of the...module groups and the memory controller are the same," as recited in independent claims 1, 8, and 15. Because Kuge fails to disclose this claim element, the rejection of independent claims 1, 8, and 15 is unwarranted and should be withdrawn.

Second, it appears that the Office Action assumes that because Kuge proposes a method for measuring the length of data transmission lines, that Kuge can actually control data transmission times. This is not true. Kuge simply uses estimated lengths of data transmission lines to estimate a "flight time" for data transmitted over the lines. (See, Kuge at column 11, lines 25-26). Kuge then uses the "flight times" to compute set up/hold times for respective memory chips in modules 1000A, 1000B, and 1000C. (See, Id). Although derived from the estimated flight times, modification of the set up/hold times does nothing to actually control the amount of time that it takes to transmit data between system controller 1 and modules 1000A, 1000B, and 1000C. Because Kuge fails to disclose N memory modules in a memory module group, where

each of the N modules has the same data transmission time to a memory controller, the rejection of independent claims 1, 8, and 15 is unwarranted and should be withdrawn.

The Office Action continues by stating that Kuge discloses "memory banks B0-B7," apparently asserting that these banks read on claims 4-5, 11-12, and 18-19. However, the Office Action fails to identify "L devices" in each bank, or appropriate data bus widths such as those defined, for example, in claims 4, 6, 11, 13, 18, or 20. Kuge simply teaches that all of banks B0-B7 are connected to a common data input/output bus G-I/O with an unspecified bit width. (See, Kuge at Fig. 8). In other words, Kuge fails to disclose most, if not all of the technical content of claims 4-5, 11-12, and 18-19 regarding bus widths, number of devices, and so on. Since Kuge fails to disclose each element of claims 4-5, 11-12, and 18-19, Kuge does not support a rejection of these claims under 35 U.S.C. § 102(b).

In conclusion, the Office Action rejected claims 1-2, 4-9, 11-16, and 18-25 under 35 U.S.C. § 102(b) as being anticipated by Kuge without showing disclosure in Kuge related to several claimed elements. Accordingly, reconsideration and a favorable action on these claims is respectfully requested.

Respectfully submitted,
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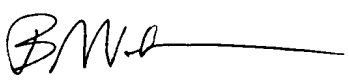

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